EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2278	(341/156,155).CCLS.	USPAT	OR	OFF	2007/01/18 09:41
L2	437	(341/156,155).CCLS.	US-PGPUB	OR	OFF	2007/01/18 09:42
L3	52	(341/156).CCLS.	US-PGPUB	OR	OFF	2007/01/18 09:42
L4	660	(analog ADJ1 digital or ad or adc) image array ampl$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/01/18 09:43
L5	100	(analog ADJ1 digital or ad or adc) image array ampl$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/01/18 09:43
L6	1	(analog ADJ1 digital or ad or adc) image array ampl$5 and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/01/18 09:44

L7	6	(analog ADJ1 digital or ad or adc) image array ampl$5 and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/01/18 09:44
L8	0	(analog ADJ1 digital or ad or adc) image array ampl$5 and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/01/18 09:44
L9	3465	(analog ADJ1 digital or ad or adc) image array	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/01/18 09:44
L10	0	(analog ADJ1 digital or ad or adc) image array and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/01/18 09:44

P⊛RTAL
USPTO

Subscribe (Full Service)

Register (Li Free)

Search: ⊙ The ACM Digital Library

+adc +image +array

THE ACM DIGITAL LIBRARY

ℹ **Feedback** **Report a prot**

Terms used **adc image array**

Sort results by |relevance ▼|
Display results |expanded form ▼|

◆ **Save results to a Binder**
❓ **Search Tips**
☐ Open results in a new window

Try an Ad
Try this s‹

Results 1 - 20 of 109   Result page: **1** <u>2</u> <u>3</u> <u>4</u> <u>5</u> <u>6</u> <u>nex</u>

1 <u>Track 6: autonomic and organic computing: Marching-pixels: a new paradigm for smart sensor processor arrays</u>
Dietmar Fey, Daniel Schmidt
May 2005 Proceedings of the 2nd conference on Computing front
Publisher: ACM Press
Full text available: 🗎 <u>pdf(606.57 KB)</u> Additional Information: <u>full citation</u>, <u>index terms</u>

> In this paper we present a new organic computing principle denoted as architectures of future smart CMOS camera chips. The idea of marching realization of a massively-parallel fine-grain single-chip processor array organic units which are propagating in a pixel processor array, similar t‹ algorithms. The task of the marching pixels is to carry out autonomousl processing tasks, e.g ...

> **Keywords**: image pre-processing, organic computing, self-organizatior smart pixels

2 <u>A 3-pin 1.5 V 550 mW 176 x 144 self-clocked CMOS active pixel im</u>
Kwang-Bo Cho, Alexander Krymski, Eric Fossum
August 2001 Proceedings of the 2001 international symposium o and design ISLPED '01
Publisher: ACM Press

Full text available: 🗎 pdf(350.69   Additional Information: <u>full citation,</u>
                         <u>KB)</u>

Keywords: CMOS, active pixel sensor, image sensor, low-power, low-v

3 <u>VLSI circuits: 40 MHz 0.25 um CMOS embedded 1T bit-line decoup</u>
◆ <u>mixed-signal applications</u>
Michael I. Fuller, James P. Mabry, John A. Hossack, Travis N. Blalock
April 2003 **Proceedings of the 13th ACM Great Lakes symposium (**
Publisher: ACM Press
Full text available: 🗎 <u>pdf(252.55</u>   Additional Information: <u>full citation,</u>
                        <u>KB)</u>   <u>index terms</u>

   An embedded 40 MHz FIFO buffer for use in mixed-signal information pi
   presented. The buffer design uses a 1T DRAM topology for its unit mem
   sense amplifier, and two circular shift registers for implementing refresh
   The sense amplifier uses bit-line decoupling to improve readout perform
   application requires the storage of 800 samples of a received ultrasound
   48 channels consisting of ...

   Keywords: CMOS, DRAM, FIFO, embedded memory, ultrasound

4 <u>Smart pixel implementation of a 2-D parallel nucleic wavelet transfor</u>
<u>communications</u>
A. M. Rassau, K. Eshraghian, H. Cheung, S. W. Lachowicz, T. C. B. Yu, W.
Wilkinson
February 1998 **Proceedings of the conference on Design, automa**
                DATE '98
Publisher: IEEE Computer Society
Full text available: 🗎 <u>pdf(75.54</u>
                        <u>KB)</u> 📑   Additional Information: <u>full citation,</u>
                        <u>Publisher</u>   <u>index terms</u>
                        <u>Site</u>

   A novel Smart Pixel Opto-VLSI architecture to implement a complete 2-
   real-time captured images is presented. The Smart Pixel architecture er
   highly parallel, compact, low power device capable of real-time capture,
   decompression and display of images suitable for Mobile Multimedia Cor

Keywords: Image Processing, Real-Time Systems, Parallel Processing, Array, Multimedia, Mobile Telecommunication

5 (Special session) presentation + poster disscussion: university desi(
real-time VGA 3-D image sensor using mixed-signal techniques
Yusuke Oike, Makoto Ikeda, Kunihiro Asada
January 2004 **Proceedings of the 2004 conference on Asia South automation: electronic design and solution fair ASI of the 2004 conference on Asia South Pacific desig design and solution fair ASP-DAC '04**

Publisher: IEEE Press

Full text available: pdf(506.41 KB) Publisher Site   Additional Information: full citation,

We have developed the first real-time 3-D image sensor with VGA pixel signal techniques to achieve high-speed and high-accuracy range calcul section method. Our mixed-signal position detector, which consists of a and time-domain approximate ADCs, provides significant information fo during high-speed analog-to-digital conversion. Moreover the position a profile of a projected be ...

6 SPOTS'06 session 4--new sensors and architectures: The low powe
processing (LEAP)embedded networked sensor system
Dustin McIntire, Kei Ho, Bernie Yip, Amarjeet Singh, Winston Wu, William
April 2006 **Proceedings of the fifth international conference on In sensor networks IPSN '06**

Publisher: ACM Press

Full text available: pdf(200.80 KB)   Additional Information: full citation, index terms

A broad range of embedded networked sensor (ENS) systems for critica applications now require complex, high peak power dissipating sensor d demand high performance computing and high bandwidth communicatic demands for these new platforms include support for computationally ir processing as well as optimization and statistical computing. To meet th while maintaining critical support for ...

Keywords: embedded wireless networked sensor, energy-aware multip

platform hardware and software architecture

7 Applications: Cyclops: in situ image sensing and interpretation in wii

Mohammad Rahimi, Rick Baer, Obimdinachi I. Iroezi, Juan C. Garcia, Jay \
Mani Srivastava

November 2005 **Proceedings of the 3rd international conference networked sensor systems SenSys '05**

Publisher: ACM Press

Full text available: pdf(1.25 MB)   Additional Information: full citation, citings, inde

Despite their increasing sophistication, wireless sensor networks still do powerful of the human senses: vision. Indeed, vision provides humans \ to distinguish objects and identify their importance. Our work seeks to p with similar capabilities by exploiting emerging, cheap, low-power and s imaging technology. In fact, we can go beyond the stereo capabilities of the large scale of ...

Keywords: CMOS imaging, imaging, power efficiency, sensor network,

8 High dynamic range imaging

Paul Debevec, Erik Reinhard, Greg Ward, Sumanta Pattanaik

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(20.22 MB)   Additional Information: full citation,

Current display devices can display only a limited range of contrast and main reasons that most image acquisition, processing, and display tech eight bits per color channel. This course outlines recent advances in hig from capture to display, that remove this restriction, thereby enabling ii color gamut and dynamic range of the original scene rather than the lim current monitor ...

9 Suffix arrays: what are they good for?

Simon J. Puglisi, William F. Smyth, Andrew Turpin

January 2006 **Proceedings of the 17th Australasian Database Cor ADC '06**

Publisher: Australian Computer Society, Inc.

Full text available: 🗎 pdf(87.76 KB)   Additional Information: full citation, index terms

Recently the theoretical community has displayed a flurry of interest in compressed suffix arrays. New, asymptotically optimal algorithms for cc compression of suffix arrays have been proposed. In this talk we will pr into the practicalities of these latest developments. In particular, we inv arrays can indeed replace inverted files, as suggested in recent literatur

10 Poster session: A single-FPGA implementation of image connected

K. Benkrid, S. Sukhsawas, D. Crookes, S. Belkacemi

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh int on Field programmable gate arrays FPGA '03**

Publisher: ACM Press

Full text available: 🗎 pdf(187.05 KB)   Additional Information: full citation,

This paper describes an architecture based on a serial iterative algorithr Component Labelling with a hardware complexity O(N) for an NxN imag scans the input image, performing a recursive non-zero maximum neigr complete forward pass is followed by an inverse pass in which the imag order. The process is repeated until no change in the image occurs. The in Handel C language and tar ...

11 Poster session: A physical retiming algorithm for field programmabl only)

Peter Suaris, Dongsheng Wang, Pei-Ning Guo, Nan-Chi Chou

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh int on Field programmable gate arrays FPGA '03**

Publisher: ACM Press

Full text available: 🗎 pdf(187.05 KB)   Additional Information: full citation,

In this paper, we present a physical retiming algorithm for sequential ci programmable gate arrays (FPGAs). This algorithm can speed up the se reducing delay of all critical paths with negative slacks. By taking advan information provided by placed circuits, this algorithm integrates two of register duplication. Retiming moves registers across combinational con duplication moves registers ac ...

12 Considerations in processing satellite images

Ronald L. Danielson

June 1980 **ACM SIGSMALL Newsletter**, Volume 6 Issue 1
Publisher: ACM Press
Full text available: 🗎 pdf(547.79 KB)   Additional Information: full citation,

Legislated demands for better control of natural resources have motivat
resource management agencies to investigate application of satellite im
management activities. The University of Santa Clara and NASA-Ames F
jointly considering the problems faced by such agencies. Advantages an
relatively small systems for the required computer processing activities
paper. In addition, summar ...

13 VLSI circuits: Design of a nanosensor array architecture
Wei Xu, N. Vijaykrishnan, Y. Xie, M. J. Irwin
April 2004 **Proceedings of the 14th ACM Great Lakes symposium (**
Publisher: ACM Press
Full text available: 🗎 pdf(1.37 MB)   Additional Information: full citation,
                                                                              index terms

This paper describes a nanowire sensor array architecture for high-spee
systems. The chip has very simple processing elements (PEs) in a mass
in which each PE is directly connected to seven sensors. A sampling rate
realized high-speed sensing feedback for electronic nose. We aim to cre
architecture, because a compact design is required ton integrate as mai
single chip. A widely used, ...

Keywords: electronic nose, gas sensing, nanowire sensor array, patter
processing

14 Recovering high dynamic range radiance maps from photographs
Paul E. Debevec, Jitendra Malik
August 1997 **Proceedings of the 24th annual conference on Comp**
interactive techniques SIGGRAPH '97
Publisher: ACM Press/Addison-Wesley Publishing Co.
Full text available: 🗎 pdf(1.43 MB)   Additional Information: full citation,
                                                                          terms

15 Towards design and validation of mixed-technology SOCs

S. Mir, B. Charlot, G. Nicolescu, P. Coste, F. Parrain, N. Zergainoh, B. Cou

March 2000 **Proceedings of the 10th Great Lakes symposium on **

Publisher: ACM Press

Full text available: pdf(581.54 Additional Information: full citation,
KB)   index terms

This paper illustrates an approach to design and validation of heterogen
emphasis is placed on devices which incorporate MEMS parts in either a
(CMOS + micromachining) SOC device, or alternatively as a hybrid syst
separate chip. The design flow is general, and it is illustrated for the cas
embedding CMOS sensors. In particular, applications based on finger-pi
considered since a ric ...

Keywords: *HDLs, MEMS, SOCs, architecture exploration, cosimulation,*

16 Exploiting FPGA-features during the emulation of a fast reactive em

Karlheinz Weiß, Thorsten Steckstor, Gernot Koch, Wolfgang Rosenstiel

February 1999 **Proceedings of the 1999 ACM/SIGDA seventh inte**
Field programmable gate arrays FPGA '99

Publisher: ACM Press

Full text available: pdf(2.02 Additional Information: full citation,
MB)   terms

17 Compilation: Automated compile-time and run-time techniques to in

MMU-less embedded systems

Lan S. Bai, Lei Yang, Robert P. Dick

October 2006 **Proceedings of the 2006 international conference c**
architecture and synthesis for embedded systems (

Publisher: ACM Press

Full text available: pdf(1.94 Additional Information: full citation,
MB)   index terms

Random access memory (RAM) is tightly-constrained in many embedde
especially true for the least expensive, lowest-power embedded system:
nodes and portable consumer electronics. The most widely-used sensor
4-10 KB of RAM and do not contain memory management units (MMUs)
implement increasingly complex applications under such tight memory (
price and power consumption constraints make ...

Keywords: data compression, embedded system, wireless sensor netw

18 Poster session: A SC-based novel configurable analog cell

Binlin Guo, Jiarong Tong

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh int on Field programmable gate arrays FPGA '03**

Publisher: ACM Press

Full text available: pdf(187.05 KB)   Additional Information: full citation,

This paper presents a high performance Configurable Analog Cell (CAC)
Basic Configurable Analog Cell (BCAC) and a digital converter block. The
for Field Programmable Analog Array (FPAA) or for Field Programmable
(FPMA). The BCAC include three innovative Programmable Switch Block
Programmable Capacitor Arrays (PCAs), and an amplifier. PSB and PCA
generate many equivalent components. In addi ...

19 A prototype VLSI chip architecture for JPEG image compression

M. Kovac, N. Ranganathan, M. Zagar

March 1995 **Proceedings of the 1995 European conference on De**

Publisher: IEEE Computer Society

Full text available: pdf(542.19 KB)
Publisher Site   Additional Information: full citation,

In this paper, we describe the design and implementation of a prototypi
architecture for implementing the JPEG baseline image compression sta
the principles of pipelining and parallelism to the maximum extent in or
and throughput. The architecture for discrete cosine transform and the
on efficient algorithms designed for high speed VLSI implementation. Th
using the Cadence tools and b ...

Keywords: 100 MHz, 1024 pixel, 1048576 pixel, CMOS digital integrati
DCT, DSP chip, JAGUAR architecture, JPEG baseline image compression
compression, VLSI, VLSI chip architecture, color images, data compress
processing chips, discrete cosine transform, discrete cosine transforms,
encoder, high speed IC, high throughput, image coding, parallel archite
processing, pipelining, prototype implementation

20 <u>SPOTS track: Networked infomechanical systems: a mobile embed</u>
<u>platform</u>
Richard Pon, Maxim A. Batalin, Jason Gordon, Aman Kansal, Duo Liu, Moh
Shirachi, Yan Yu, Mark Hansen, William J. Kaiser, Mani Srivastava, Gaurav
April 2005 **Proceedings of the 4th international symposium on Inf**
sensor networks IPSN '05

Publisher: IEEE Press

Full text available: <u>pdf(365.69 KB)</u>   Additional Information: <u>full citation,</u>

Networked Infomechanical Systems (NIMS) introduces a new actuation
networked sensing. By exploiting a constrained actuation method based
infrastructure, NIMS suspends a network of wireless mobile and fixed se
dimensional space. This permits run-time adaptation with variable sensi
and even sensor type. Discoveries in NIMS environmental investigations
for 1) new embedded platforms int ...

Keywords: actuation, embedded, mobility, networked, sensor, system

Results 1 - 20 of 109   Result page: **1** <u>2</u> <u>3</u> <u>4</u> <u>5</u> <u>6</u> <u>nex</u>

⊚ P❀RTAL
USPTO

Search: ⊚ The ACM Digital Library

+adc +imaging +array

THE ACM DIGITAL LIBRARY

ℹ Feedback   Report a prot

Terms used **adc imaging array**

Sort results by relevance ▽
Display results expanded form ▽

❖ Save results to a Binder   Try an Ad
❓ Search Tips   Try this s⟨
☐ Open results in a new window

Results 1 - 20 of 109   Result page: **1** <u>2</u> <u>3</u> <u>4</u> <u>5</u> <u>6</u>   <u>nex</u>

1 <u>Track 6: autonomic and organic computing: Marching-pixels: a new paradigm for smart sensor processor arrays</u>
Dietmar Fey, Daniel Schmidt
May 2005 **Proceedings of the 2nd conference on Computing front**
Publisher: ACM Press
Full text available: 📄 <u>pdf(606.57 KB)</u>   Additional Information: <u>full citation,</u> <u>index terms</u>

In this paper we present a new organic computing principle denoted as architectures of future smart CMOS camera chips. The idea of marching realization of a massively-parallel fine-grain single-chip processor array organic units which are propagating in a pixel processor array, similar t⟨ algorithms. The task of the marching pixels is to carry out autonomousl processing tasks, e.g ...

Keywords: image pre-processing, organic computing, self-organizatior smart pixels

2 <u>A 3-pin 1.5 V 550 mW 176 x 144 self-clocked CMOS active pixel im</u>
Kwang-Bo Cho, Alexander Krymski, Eric Fossum
August 2001 **Proceedings of the 2001 international symposium o and design ISLPED '01**
Publisher: ACM Press

Full text available: 📄 pdf(350.69 Additional Information: full citation,
                              KB)

Keywords: CMOS, active pixel sensor, image sensor, low-power, low-v

3 VLSI circuits: 40 MHz 0.25 um CMOS embedded 1T bit-line decoup
mixed-signal applications
Michael I. Fuller, James P. Mabry, John A. Hossack, Travis N. Blalock
April 2003 **Proceedings of the 13th ACM Great Lakes symposium c**
Publisher: ACM Press
Full text available: 📄 pdf(252.55 Additional Information: full citation,
                              KB)   index terms

> An embedded 40 MHz FIFO buffer for use in mixed-signal information pi
> presented. The buffer design uses a 1T DRAM topology for its unit mem
> sense amplifier, and two circular shift registers for implementing refresh
> The sense amplifier uses bit-line decoupling to improve readout perform
> application requires the storage of 800 samples of a received ultrasound
> 48 channels consisting of ...

Keywords: CMOS, DRAM, FIFO, embedded memory, ultrasound

4 Smart pixel implementation of a 2-D parallel nucleic wavelet transfor
communications
A. M. Rassau, K. Eshraghian, H. Cheung, S. W. Lachowicz, T. C. B. Yu, W.
Wilkinson
February 1998 **Proceedings of the conference on Design, automa
                      DATE '98**
Publisher: IEEE Computer Society
Full text available: 📄 pdf(75.54
                              KB) 📰   Additional Information: full citation,
                              Publisher   index terms
                              Site

> A novel Smart Pixel Opto-VLSI architecture to implement a complete 2-
> real-time captured images is presented. The Smart Pixel architecture er
> highly parallel, compact, low power device capable of real-time capture,
> decompression and display of images suitable for Mobile Multimedia Cor

Keywords: Image Processing, Real-Time Systems, Parallel Processing, Array, Multimedia, Mobile Telecommunication

5 (Special session) presentation + poster disscussion: university desi(
real-time VGA 3-D image sensor using mixed-signal techniques
Yusuke Oike, Makoto Ikeda, Kunihiro Asada
January 2004 **Proceedings of the 2004 conference on Asia South
automation: electronic design and solution fair ASH
of the 2004 conference on Asia South Pacific desig
design and solution fair ASP-DAC '04**

Publisher: IEEE Press

Full text available: pdf(506.41
KB)
Publisher
Site   Additional Information: full citation,

We have developed the first real-time 3-D image sensor with VGA pixel
signal techniques to achieve high-speed and high-accuracy range calcul
section method. Our mixed-signal position detector, which consists of a
and time-domain approximate ADCs, provides significant information fo
during high-speed analog-to-digital conversion. Moreover the position a
profile of a projected be ...

6 SPOTS'06 session 4--new sensors and architectures: The low powe
processing (LEAP)embedded networked sensor system
Dustin McIntire, Kei Ho, Bernie Yip, Amarjeet Singh, Winston Wu, William
April 2006 **Proceedings of the fifth international conference on In
sensor networks IPSN '06**

Publisher: ACM Press

Full text available: pdf(200.80 Additional Information: full citation,
KB)   index terms

A broad range of embedded networked sensor (ENS) systems for critica
applications now require complex, high peak power dissipating sensor d
demand high performance computing and high bandwidth communicati(
demands for these new platforms include support for computationally ir
processing as well as optimization and statistical computing. To meet th
while maintaining critical support for ...

Keywords: embedded wireless networked sensor, energy-aware multi[

platform hardware and software architecture

7 Applications: Cyclops: in situ image sensing and interpretation in wii

Mohammad Rahimi, Rick Baer, Obimdinachi I. Iroezi, Juan C. Garcia, Jay \
Mani Srivastava

November 2005 **Proceedings of the 3rd international conference networked sensor systems SenSys '05**

Publisher: ACM Press

Full text available: 🗎 pdf(1.25 MB)   Additional Information: full citation, citings, inde

Despite their increasing sophistication, wireless sensor networks still do
powerful of the human senses: vision. Indeed, vision provides humans ∨
to distinguish objects and identify their importance. Our work seeks to ⌡
with similar capabilities by exploiting emerging, cheap, low-power and ꜱ
imaging technology. In fact, we can go beyond the stereo capabilities oʃ
the large scale of ...

Keywords: CMOS imaging, imaging, power efficiency, sensor network,

8 High dynamic range imaging

Paul Debevec, Erik Reinhard, Greg Ward, Sumanta Pattanaik

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: 🗎 pdf(20.22 MB)   Additional Information: full citation,

Current display devices can display only a limited range of contrast and
main reasons that most image acquisition, processing, and display tech
eight bits per color channel. This course outlines recent advances in hig
from capture to display, that remove this restriction, thereby enabling iₗ
color gamut and dynamic range of the original scene rather than the lim
current monitor ...

9 Suffix arrays: what are they good for?

Simon J. Puglisi, William F. Smyth, Andrew Turpin

January 2006 **Proceedings of the 17th Australasian Database Coɪ ADC '06**

Publisher: Australian Computer Society, Inc.

Full text available: 📄 pdf(87.76 KB)   Additional Information: <u>full citation,</u> <u>index terms</u>

Recently the theoretical community has displayed a flurry of interest in compressed suffix arrays. New, asymptotically optimal algorithms for cc compression of suffix arrays have been proposed. In this talk we will pr into the practicalities of these latest developments. In particular, we inv arrays can indeed replace inverted files, as suggested in recent literatur

10 <u>Poster session: A single-FPGA implementation of image connected</u>
K. Benkrid, S. Sukhsawas, D. Crookes, S. Belkacemi
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh int on Field programmable gate arrays FPGA '03**

Publisher: ACM Press

Full text available: 📄 <u>pdf(187.05 KB)</u>   Additional Information: <u>full citation,</u>

This paper describes an architecture based on a serial iterative algorithr Component Labelling with a hardware complexity $O(N)$ for an NxN imag scans the input image, performing a recursive non-zero maximum neigl complete forward pass is followed by an inverse pass in which the imag order. The process is repeated until no change in the image occurs. The in Handel C language and tar ...

11 <u>Poster session: A physical retiming algorithm for field programmable</u>
<u>only)</u>
Peter Suaris, Dongsheng Wang, Pei-Ning Guo, Nan-Chi Chou
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh int on Field programmable gate arrays FPGA '03**

Publisher: ACM Press

Full text available: 📄 <u>pdf(187.05 KB)</u>   Additional Information: <u>full citation,</u>

In this paper, we present a physical retiming algorithm for sequential ci programmable gate arrays (FPGAs). This algorithm can speed up the se reducing delay of all critical paths with negative slacks. By taking advan information provided by placed circuits, this algorithm integrates two of register duplication. Retiming moves registers across combinational con duplication moves registers ac ...

12 <u>Considerations in processing satellite images</u>
Ronald L. Danielson

June 1980 **ACM SIGSMALL Newsletter,** Volume 6 Issue 1
Publisher: ACM Press
Full text available: pdf(547.79 KB)   Additional Information: full citation,

Legislated demands for better control of natural resources have motivat
resource management agencies to investigate application of satellite im
management activities. The University of Santa Clara and NASA-Ames F
jointly considering the problems faced by such agencies. Advantages an
relatively small systems for the required computer processing activities
paper. In addition, summar ...

13 VLSI circuits: Design of a nanosensor array architecture
Wei Xu, N. Vijaykrishnan, Y. Xie, M. J. Irwin
April 2004 **Proceedings of the 14th ACM Great Lakes symposium o**
Publisher: ACM Press
Full text available: pdf(1.37 MB)   Additional Information: full citation,
index terms

This paper describes a nanowire sensor array architecture for high-spee
systems. The chip has very simple processing elements (PEs) in a mass
in which each PE is directly connected to seven sensors. A sampling rate
realized high-speed sensing feedback for electronic nose. We aim to cre
architecture, because a compact design is required ton integrate as mai
single chip. A widely used, ...

Keywords: electronic nose, gas sensing, nanowire sensor array, patter
processing

14 Recovering high dynamic range radiance maps from photographs
Paul E. Debevec, Jitendra Malik
August 1997 **Proceedings of the 24th annual conference on Comp**
interactive techniques SIGGRAPH '97
Publisher: ACM Press/Addison-Wesley Publishing Co.
Full text available: pdf(1.43 MB)   Additional Information: full citation,
terms

15 Towards design and validation of mixed-technology SOCs

S. Mir, B. Charlot, G. Nicolescu, P. Coste, F. Parrain, N. Zergainoh, B. Cou
March 2000 **Proceedings of the 10th Great Lakes symposium on **
Publisher: ACM Press
Full text available: 📄 pdf(581.54   Additional Information: full citation,
              KB)   index terms

> *This paper illustrates an approach to design and validation of heterogen*
> *emphasis is placed on devices which incorporate MEMS parts in either a*
> *(CMOS + micromachining) SOC device, or alternatively as a hybrid syst*
> *separate chip. The design flow is general, and it is illustrated for the cas*
> *embedding CMOS sensors. In particular, applications based on finger-pi*
> *considered since a ric ...*

> **Keywords:** *HDLs, MEMS, SOCs, architecture exploration, cosimulation,*

16 Exploiting FPGA-features during the emulation of a fast reactive em
Karlheinz Weiß, Thorsten Steckstor, Gernot Koch, Wolfgang Rosenstiel
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh inte**
              Field programmable gate arrays FPGA '99
Publisher: ACM Press
Full text available: 📄 pdf(2.02   Additional Information: full citation,
              MB)   terms

17 Compilation: Automated compile-time and run-time techniques to in
MMU-less embedded systems
Lan S. Bai, Lei Yang, Robert P. Dick
October 2006 **Proceedings of the 2006 international conference (**
              architecture and synthesis for embedded systems (
Publisher: ACM Press
Full text available: 📄 pdf(1.94   Additional Information: full citation,
              MB)   index terms

> Random access memory (RAM) is tightly-constrained in many embedde
> especially true for the least expensive, lowest-power embedded system
> nodes and portable consumer electronics. The most widely-used sensor
> 4-10 KB of RAM and do not contain memory management units (MMUs)
> implement increasingly complex applications under such tight memory (
> price and power consumption constraints make ...

Keywords: data compression, embedded system, wireless sensor netw

18 Poster session: A SC-based novel configurable analog cell

Binlin Guo, Jiarong Tong

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh int
on Field programmable gate arrays FPGA '03**

Publisher: ACM Press

Full text available: pdf(187.05 KB)   Additional Information: full citation,

This paper presents a high performance Configurable Analog Cell (CAC)
Basic Configurable Analog Cell (BCAC) and a digital converter block. The
for Field Programmable Analog Array (FPAA) or for Field Programmable
(FPMA). The BCAC include three innovative Programmable Switch Block
Programmable Capacitor Arrays (PCAs), and an amplifier. PSB and PCA
generate many equivalent components. In addi ...

19 A prototype VLSI chip architecture for JPEG image compression

M. Kovac, N. Ranganathan, M. Zagar

March 1995 **Proceedings of the 1995 European conference on De:**

Publisher: IEEE Computer Society

Full text available: pdf(542.19 KB)
Publisher Site   Additional Information: full citation,

In this paper, we describe the design and implementation of a prototype
architecture for implementing the JPEG baseline image compression sta
the principles of pipelining and parallelism to the maximum extent in or
and throughput. The architecture for discrete cosine transform and the
on efficient algorithms designed for high speed VLSI implementation. Th
using the Cadence tools and b ...

Keywords: 100 MHz, 1024 pixel, 1048576 pixel, CMOS digital integrat
DCT, DSP chip, JAGUAR architecture, JPEG baseline image compression
compression, VLSI, VLSI chip architecture, color images, data compres:
processing chips, discrete cosine transform, discrete cosine transforms,
encoder, high speed IC, high throughput, image coding, parallel archite
processing, pipelining, prototype implementation

20 <u>SPOTS track: Networked infomechanical systems: a mobile embed</u>
<u>platform</u>
Richard Pon, Maxim A. Batalin, Jason Gordon, Aman Kansal, Duo Liu, Moh
Shirachi, Yan Yu, Mark Hansen, William J. Kaiser, Mani Srivastava, Gaurav
April 2005 **Proceedings of the 4th international symposium on Inf**
sensor networks IPSN '05
Publisher: IEEE Press
Full text available: 🗎 <u>pdf(365.69</u>
<u>KB)</u> Additional Information: <u>full citation,</u>

Networked Infomechanical Systems (NIMS) introduces a new actuation–
networked sensing. By exploiting a constrained actuation method based
infrastructure, NIMS suspends a network of wireless mobile and fixed se
dimensional space. This permits run-time adaptation with variable sensi
and even sensor type. Discoveries in NIMS environmental investigations
for 1) new embedded platforms int ...

Keywords: actuation, embedded, mobility, networked, sensor, system

Results 1 - 20 of 109 Result page: **1** 2 3 4 5 6 nex

PORTAL
USPTO

Search: ⊙ The ACM Digital Library

`+analog +digital +imaging +array`

🛈 **Feedback** **Report a prol**

Terms used **analog digital imaging array**

Sort results by `relevance` ▼
Display results `expanded form` ▼

❧ Save results to a Binder
❓ Search Tips
☐ Open results in a new window

Try an Ad
Try this s∈

Results 1 - 20 of 200   Result page: **1** 2 3 4 5 6 7 8 9 1
Best 200 shown

1 Layout tools for analog ICs and mixed-signal SoCs: a survey
Rob A. Rutenbar, John M. Cohn
May 2000 **Proceedings of the 2000 international symposium on P**
Publisher: ACM Press
Full text available: 📄 pdf(247.03 KB)   Additional Information: full citation,

2 (Special session) presentation + poster disscussion: university desi(
real-time VGA 3-D image sensor using mixed-signal techniques
Yusuke Oike, Makoto Ikeda, Kunihiro Asada
January 2004 **Proceedings of the 2004 conference on Asia South**
automation: electronic design and solution fair ASI
of the 2004 conference on Asia South Pacific desig
design and solution fair ASP-DAC '04
Publisher: IEEE Press
Full text available: 📄 pdf(506.41 KB) 📑
Publisher Site   Additional Information: full citation,

We have developed the first real-time 3-D image sensor with VGA pixel
signal techniques to achieve high-speed and high-accuracy range calcul
section method. Our mixed-signal position detector, which consists of ai

and time-domain approximate ADCs, provides significant information fo
during high-speed analog-to-digital conversion. Moreover the position a
profile of a projected be ...

3 "Empty space" computes: the evolution of an unconventional superc
Jonathan W. Mills, Matt Parker, Bryce Himebaugh, Craig Shue, Brian Kope
May 2006 **Proceedings of the 3rd conference on Computing fronti**
Publisher: ACM Press
Full text available: pdf(1.82   Additional Information: full citation,
                MB)   index terms

Lee A. Rubel defined the extended analog computer to avoid the limitati
purpose analog computer. Partial differential equation solvers were a "q
Rubel's theoretical machine. These components have been implemented
VLSI circuits without transistors, as well as conductive plastic. For the p
Indiana University has explored the design and applications of extendec
machines have become incre ...

Keywords: Lukasiewicz logic, extended analog computer, general purp
hybrid digital-analog architecture

4 Personal imaging and lookpainting as tools for personal documentar
photojournalism
Steve Mann
March 1999 **Mobile Networks and Applications,** Volume 4 Issue 1
Publisher: Kluwer Academic Publishers
Full text available: pdf(2.24   Additional Information: full citation,
                MB)   citings, inde

A means and apparatus for covert capture of extremely high-resolution
presented. The apparatus embodies a new form of user-interface – inst
and click" metaphor which was thought to be the simplest photography
proposed is a "look" metaphor in which images are generated through t
looking around, in a manner that does not require conscious thought or

5 A 3-pin 1.5 V 550 mW 176 x 144 self-clocked CMOS active pixel im
Kwang-Bo Cho, Alexander Krymski, Eric Fossum
August 2001 **Proceedings of the 2001 international symposium o
and design ISLPED '01**
Publisher: ACM Press

Full text available: 📄 pdf(350.69 Additional Information: full citation,
KB)

Keywords: CMOS, active pixel sensor, image sensor, low-power, low-v

6 Reviewed papers: Using image processing to teach CS1 and CS2
Kenny Hunt
December 2003 **ACM SIGCSE Bulletin**, Volume 35 Issue 4
Publisher: ACM Press
Full text available: 📄 pdf(676.87 Additional Information: full citation,
KB)   citings

The use of digital image processing techniques in undergraduate compu
advantages in terms of motivating student interest and immediate, visu
code. Although the standard Java distribution includes support for basic
operations, including the display of images, the complexity of the packa
inexperienced programmers. This paper presents an extension to the bu
package that is suitable f ...

7 High performance imaging using large camera arrays
Bennett Wilburn, Neel Joshi, Vaibhav Vaish, Eino-Ville Talvala, Emilio Antu
Adams, Mark Horowitz, Marc Levoy
July 2005 **ACM Transactions on Graphics (TOG) , ACM SIGGRAPH
'05**, Volume 24 Issue 3
Publisher: ACM Press
Full text available: 📄 pdf(902.47
KB) 🎬 mov   Additional Information: full citation,
(21:45 MIN)   citings, inde

The advent of inexpensive digital image sensors and the ability to creat
information from a number of sensed images are changing the way we
In this paper, we describe a unique array of 100 custom video cameras
summarize our experiences using this array in a range of imaging applic
explore the capabilities of a system that would be inexpensive to produ
mind, we used s ...

Keywords: camera arrays, spatiotemporal sampling, synthetic apertur

8 High dynamic range imaging

Paul Debevec, Erik Reinhard, Greg Ward, Sumanta Pattanaik

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(20.22 MB)   Additional Information: full citation,

Current display devices can display only a limited range of contrast and
main reasons that most image acquisition, processing, and display techi
eight bits per color channel. This course outlines recent advances in hig
from capture to display, that remove this restriction, thereby enabling ii
color gamut and dynamic range of the original scene rather than the lim
current monitor ...

9 Scanned-display computer graphics

A. Michael Noll

March 1971 **Communications of the ACM**, Volume 14 Issue 3

Publisher: ACM Press

Full text available: pdf(781.96 KB)   Additional Information: full citation, citings

A television-like scanned-display system has been successfully impleme
224 computer installation. The scanned image is stored in the core men
software scan conversion is used to convert the rectangular coordinates
appropriate word and bit in an output display array in core storage. Res
flicker-free displays of large amounts of data are possible with reasonat
interaction. A scanned im ...

Keywords: computer graphics, raster displays, scan conversion, scann

10 Applications: Cyclops: in situ image sensing and interpretation in wii

Mohammad Rahimi, Rick Baer, Obimdinachi I. Iroezi, Juan C. Garcia, Jay \
Mani Srivastava

November 2005 **Proceedings of the 3rd international conference networked sensor systems SenSys '05**

Publisher: ACM Press

Full text available: pdf(1.25 MB)   Additional Information: full citation, citings, inde

Despite their increasing sophistication, wireless sensor networks still do

powerful of the human senses: vision. Indeed, vision provides humans \
to distinguish objects and identify their importance. Our work seeks to \
with similar capabilities by exploiting emerging, cheap, low-power and s
imaging technology. In fact, we can go beyond the stereo capabilities of
the large scale of ...

Keywords: CMOS imaging, imaging, power efficiency, sensor network,

11 Progress in Picture Processing: 1969--71

Azriel Rosenfeld

June 1973 **ACM Computing Surveys (CSUR)**, Volume 5 Issue 2

Publisher: ACM Press

Full text available: pdf(2.34 MB)   Additional Information: full citation, terms

12 An on-line image processing system

I. H. Barkdoll, B. L. McGlamery

January 1968 **Proceedings of the 1968 23rd ACM national confere**

Publisher: ACM Press

Full text available: pdf(2.04 MB)   Additional Information: full citation,

The high-speed digital computer has contributed to significant progress
particular area of optics benefiting from this progress is image processir
processing is to aid the human observer in extracting from an image inf
obscured by some type of degradation The numerous factors which can
image in an optical system include lens aberrations, poor focus, image r
di ...

13 MAPS: a generalized image processor

Michael Fischer

September 1973 **ACM SIGGRAPH Computer Graphics**, Volume 7 Is:

Publisher: ACM Press

Full text available: pdf(769.35 KB)   Additional Information: full citation,

By approaching two and three-dimensional problems from the spatial vi
geographic sciences, the <u>M</u>ulti-dimensional <u>A</u>nalysis

<u>S</u>ystem (MAPS) is able to achieve high efficiency and large ca|
interactive graphics, simulation modeling, and image processing. Spatia
presented by means of color images, rather than line drawings, facilitat

14 Track 6: autonomic and organic computing: Marching-pixels: a new paradigm for smart sensor processor arrays
Dietmar Fey, Daniel Schmidt
May 2005 **Proceedings of the 2nd conference on Computing front**
Publisher: ACM Press
Full text available: pdf(606.57 KB) Additional Information: full citation, index terms

In this paper we present a new organic computing principle denoted as architectures of future smart CMOS camera chips. The idea of marching realization of a massively-parallel fine-grain single-chip processor array organic units which are propagating in a pixel processor array, similar t(algorithms. The task of the marching pixels is to carry out autonomousl processing tasks, e.g ...

Keywords: image pre-processing, organic computing, self-organizatior smart pixels

15 Inexpensive real-time image generation and control
Bill Etra, Lou Katz
April 1977 **ACM SIGGRAPH Computer Graphics,** Volume 11 Issue 1
Publisher: ACM Press
Full text available: pdf(603.12 KB) Additional Information: full citation,

16 TPphotoSuite: a windows based digital image processing program
Tauhida Parveen
January 2004 **Journal of Computing Sciences in Colleges,** Volume
Publisher: Consortium for Computing Sciences in Colleges
Full text available: pdf(184.78 KB) Additional Information: full citation, index terms

The purpose of this paper is to present a Windows based software tool r capable of performing image-processing operations. *TPphotoSuite* is fre

compatible platform, the existing image processing operations can be m
operations can be added to it. *TPphotoSuite* provides a user-friendly GU
computer literacy for it to use. It contains many features that are used
as, colo ...

17 Three-dimensional medical imaging: algorithms and computer syste

M. R. Stytz, G. Frieder, O. Frieder

December 1991 **ACM Computing Surveys (CSUR)**, Volume 23 Issue

Publisher: ACM Press

Full text available: pdf(7.38 MB) Additional Information: full citation, terms, revie'

Keywords: Computer graphics, medical imaging, surface rendering, th
volume rendering

18 Cellular wave computers and CNN technology - a SoC architecture
sensor arrays

T. Roska

May 2005 **Proceedings of the 2005 IEEE/ACM International confe
aided design ICCAD '05**

Publisher: IEEE Computer Society

Full text available: pdf(415.00 KB) Additional Information: full citation,

Cellular wave computers and cellular nonlinear network (CNN) technolo
paper. It is a system-on-chip (SoC) architecture with xK processors and
architectural lessons from the trends in manufacturing billion componen
the threshold of 100 nm feature size will determine the architecture, the
and the type of algorithms needed, hence also the complexity of the sol

19 Anti-aliasing in topological color spaces

Kenneth Turkowski

August 1986 **ACM SIGGRAPH Computer Graphics , Proceedings of
conference on Computer graphics and interactive te
'86**, Volume 20 Issue 4

Publisher: ACM Press

Full text available: pdf(5.19   Additional Information: full citation,

MB)   index terms

The power of a color space to perform well in interpolation problems su(
smooth-shading is dependent on the topology of the color space as well
it contains.We develop the *Major-minor* color space, which has a topolo(
lends itself to simple anti-aliasing computations between elements of ar
an inexpensive frame store.

20 Bio-Inspired Analog VLSI Design Realizes Programmable Complex
Dynamics on a Single Chip
R. Carmona, F. Jiménez-Garrido, R. Domínguez-Castro, S. Espejo, A. Rodí
March 2002 **Proceedings of the conference on Design, automatioi
DATE '02**
Publisher: IEEE Computer Society
Full text available: pdf(4.22
MB)   Additional Information: full citation,

A bio-inspired model for an analog parallel array pro-cessor(APAP), bas(
vertebrate retina,permits the realization of complex spatio-temporal dyi
mimics the way in which imagesare processed in the visual pathway wh
feasiblealternative for the implementation of early vision tasks instanda
prototype chip has been designedin 0.5μm CMOS. Design challenges, tr
blocks of such a high-complexity system(0.5 ...

Results 1 - 20 of 200   Result page: **1**   2   3   4   5   6   7   8